Bi-weekly Status Report 1
Senior Design, December 2020, Team 14

Introduction of Real-World Signals and Systems into ECpE DSP Laboratory Curriculum

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Progress Summary:
Over the past two weeks, the team has been getting back up to speed and mapping out the plan of the rest of the semester. We have started establishing new weekly items and goals to help us be successful with output and time management. We have made progress on the CyDAQ firmware and GUI front end, started solidifying major hardware design updates, and began wrapping up EE 224 labs and outlining EE 324 labs.

Individual Contributions by Team Member:

- **Brady Anderson (Biweekly: 12; Cumulative: 12)**
  - Created CyDAQ firmware boot image
    - Installed boot image on SD cards and distributed to ETG
  - Debugged serial communication interface
  - Installed FreeRTOS demo implementation
  - Began considering strategies for mapping CyDAQ firmware to FreeRTOS parallel tasks
- **Sam Burnett (Bi-weekly: 12, Cumulative: 12)**
  - Drafted part comparison sheet for external ADC
  - Simulated pass-through bandwidth of front end FDA
  - Designed schematic for 3MHz analog front-end
  - Designed evaluation module board layout for analog front-end
- **Mitchell Hoppe (Weekly: 12; Cumulative: 74.0)**
  - Updated the website to improve the design of the Teams page
  - Worked on the front-end to improve the usability
  - Worked to connect the front-end Matlab with the python to communicate with the CyDaq
- **Max Kiley (Biweekly: 10; Cumulative: 10)**
  - Began learning how to implement FreeRTOS onto the CyDAQ firmware
  - Researched resource scheduling and synchronization using semaphores and mutexes
  - Read-up on EE 324 learning objectives and previous labs
- **Emily LaGrant (Biweekly: 14; Cumulative: 79)**
  - Read-up on EE 324 course and lab objectives
  - Brainstormed and researched potential lab topics
  - Decided on finalized list of labs to create this semester
  - Began writing a rough draft for heart rate sensor design lab for EE224

- **Isaac Rex (Bi-Weekly: 15; Cumulative:15)**
    - Scheduled weekly meetings with advisor
    - Wrote two complete lab outlines
    - Began working on circuit for EE 324 controls lab
    - Began simulations for EE 324 controls lab

Pending Issues:

- There are currently no pending issues

Plans:

- Isaac:
    - Finalize circuit for power supply controls lab
    - Finish simulations and derive formula
    - Begin writing MATLAB solution code for controls lab
- Emily:
    - Continue adding to rough draft of EE 224 heart rate project lab
    - Begin rough draft of EE 324 labs
    - Test heart rate project lab
- Brady:
    - Create FreeRTOS tasks for CyDAQ firmware functions
    - Review communication standard and consider possible improvements
    - Test Sam's PWM intuition lab with prototype PMOD
- Sam:
    - Complete design review for analog front-end
    - Order evaluation module boards for external ADC with FDA driver
    - Validate SPI block functionality
- Max
    - Continue to research FreeRTOS implementation
    - Begin working on implementation of Semaphores API
- Mitch
    - Continue work on integrating the Matlab GUI with the existing python code
    - Continue to improve the design of the website.